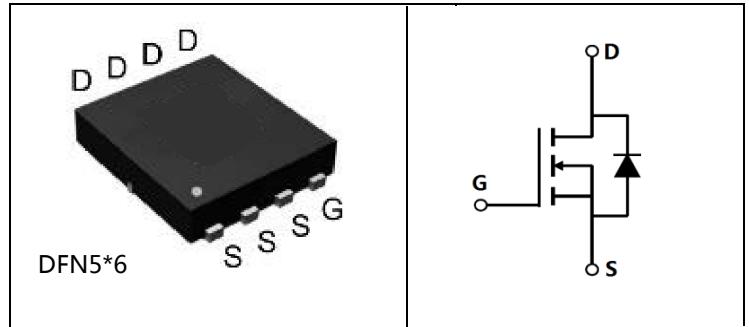


Features

- $BV_{DSS}=100\text{ V}$, $I_D=94\text{ A}$
- $R_{DS(on)}:6.5\text{ m}\Omega$ (Max) @ $V_{GS}=10\text{ V}$
- $R_{DS(on)}:9\text{ m}\Omega$ (Max) @ $V_{GS}=4.5\text{ V}$
- N-Channel, 5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- 100% Avalanche test



Device Marking and Package Information

Ordering code	Package	Marking
MPGJ10R7	DFN5*6	MPGJ10R7

Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C=25^\circ\text{C}$ 94	A
I_D	Continuous drain current @ $V_{GS}=10\text{ V}$	$T_C=25^\circ\text{C}$ 94	A
		$T_C=100^\circ\text{C}$ 67	A
I_{DM}	Pulse drain current tested ①	$T_C=25^\circ\text{C}$ 376	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{ V}$	$T_A=25^\circ\text{C}$ 10	A
		$T_A=70^\circ\text{C}$ 8	A
EAS	Avalanche energy, single pulsed ②	41	mJ
P_D	Maximum power dissipation	$T_C=25^\circ\text{C}$ 139	W
P_{DSM}	Maximum power dissipation ③	$T_A=25^\circ\text{C}$ 1.25	W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	$^\circ\text{C/W}$



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	--	2.3	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =20A	--	5.2	6.5	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =15A	--	7.0	9.0	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	--	2945	--	pF
C _{oss}	Output Capacitance		--	950	--	pF
C _{rss}	Reverse Transfer Capacitance		--	100	--	pF
R _g	Gate Resistance	f=1MHz	--	1	--	Ω
Q _g	Total Gate Charge	V _{DS} =50V, I _D =20A, V _{GS} =10V	--	50	--	nC
Q _{gs}	Gate-Source Charge		--	6	--	nC
Q _{gd}	Gate-Drain Charge		--	10	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =20A, R _G =3Ω, V _{GS} =10V	--	11.7	--	ns
t _r	Turn-on Rise Time		--	7.2	--	ns
t _{d(off)}	Turn-Off Delay Time		--	34.5	--	ns
t _f	Turn-Off Fall Time		--	12.3	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =20A, V _{GS} =0V	--	0.8	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =20A, V _{GS} =0V di/dt=500A/μs	--	21.6	--	ns
Q _{rr}	Reverse Recovery Charge		--	44.7	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 10A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycles ≤ 2%.

Typical Characteristics

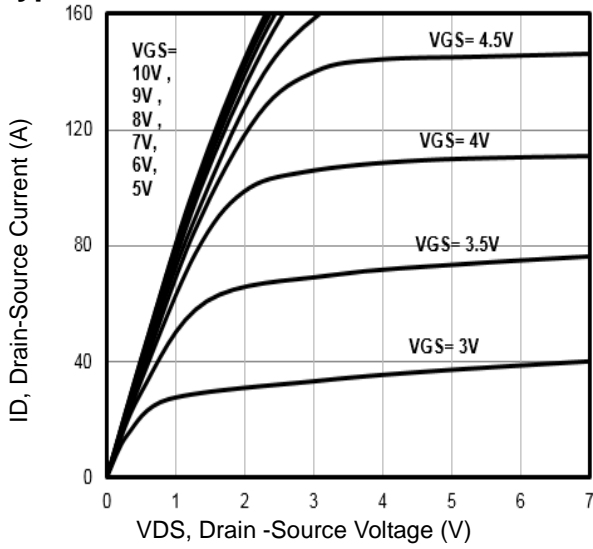


Fig1. Typical Output Characteristics

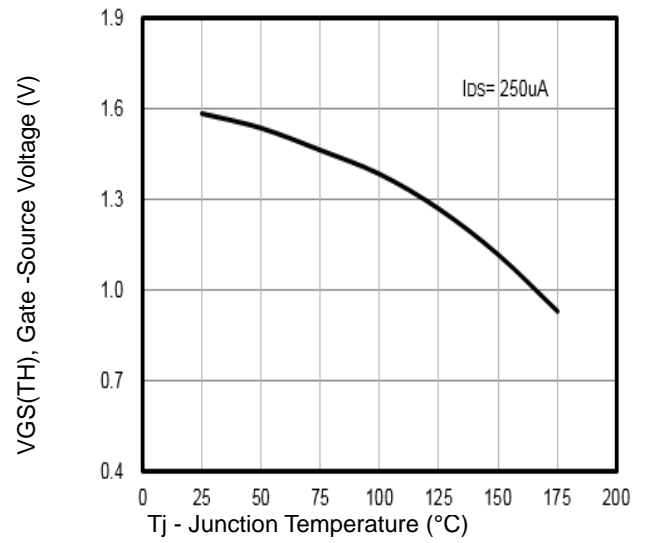


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

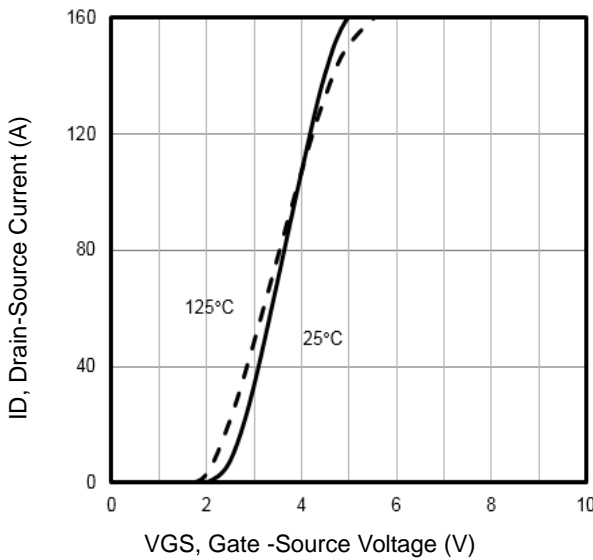


Fig3. Typical Transfer Characteristics

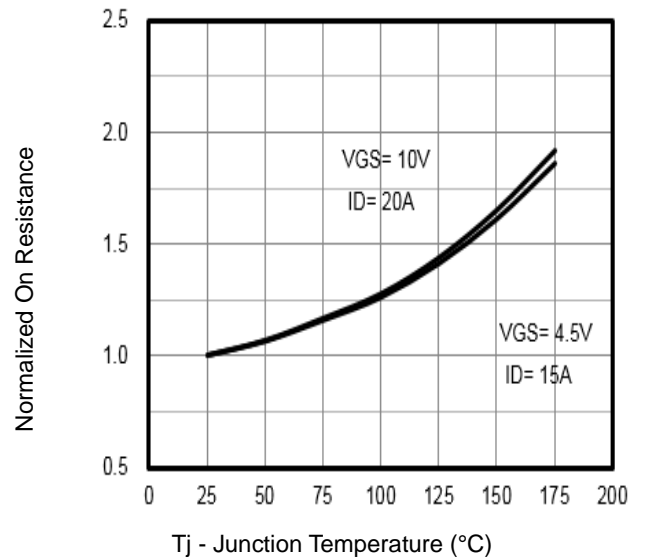


Fig4. Normalized On-Resistance Vs. T_j

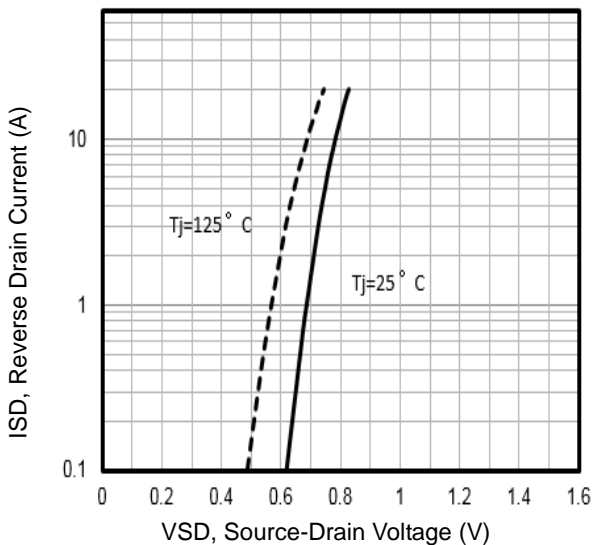


Fig5. Typical Source-Drain Diode Forward Voltage

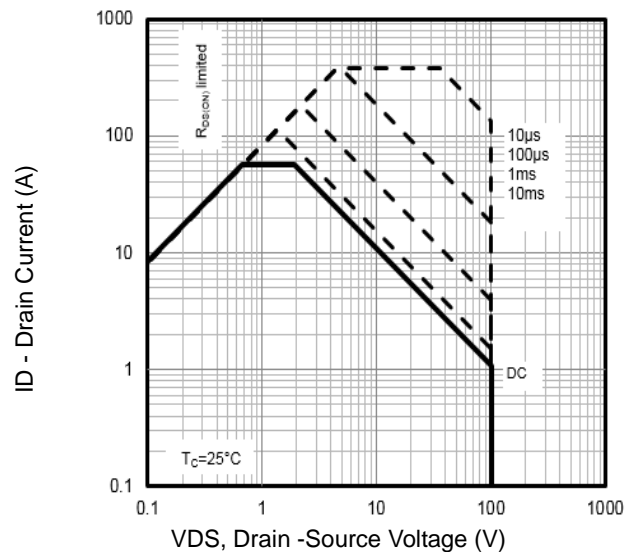


Fig6. Maximum Safe Operating Area

Typical Characteristics

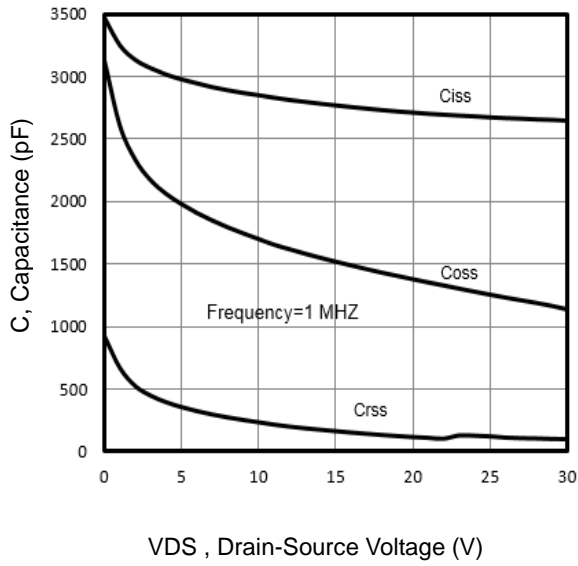


Fig7. Typical Capacitance Vs. Drain-Source Voltage

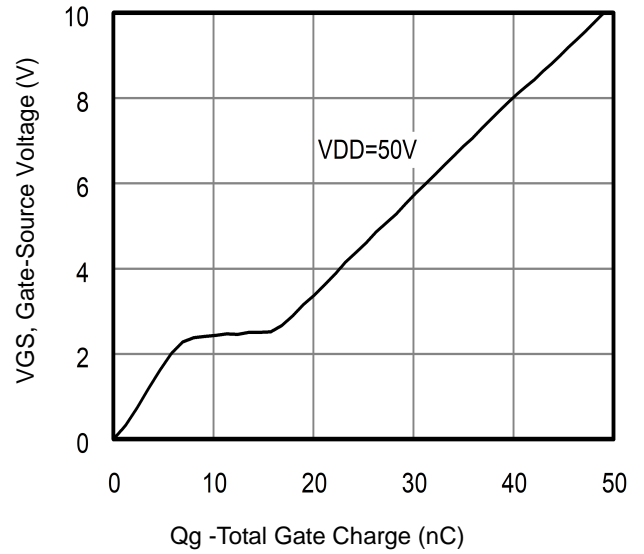


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

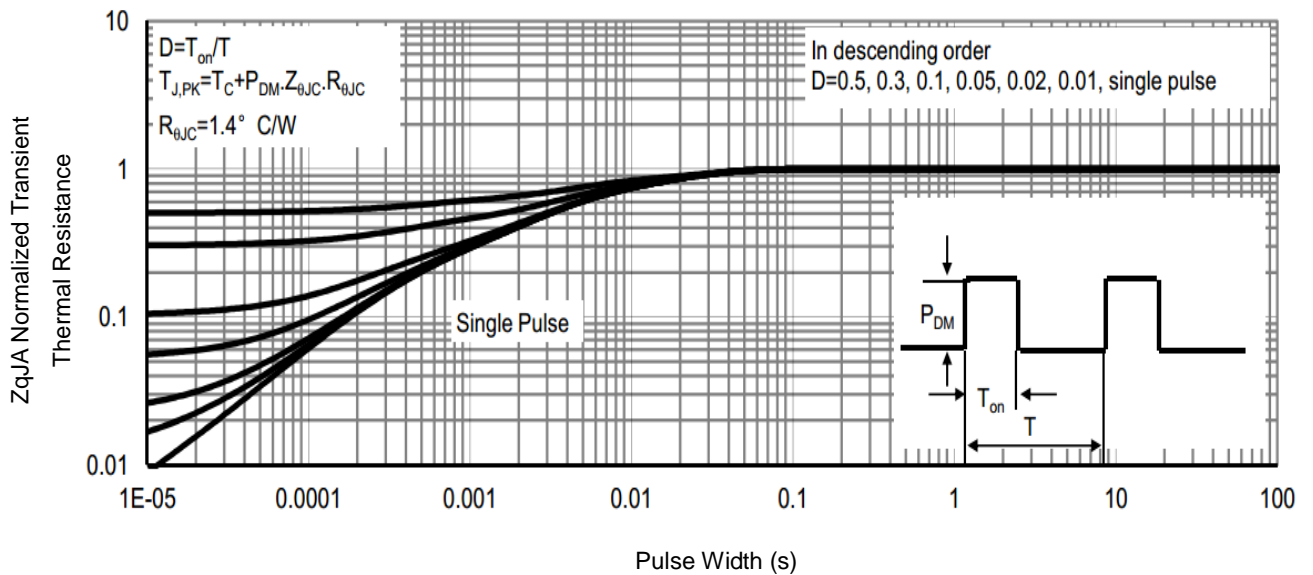


Fig9. Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

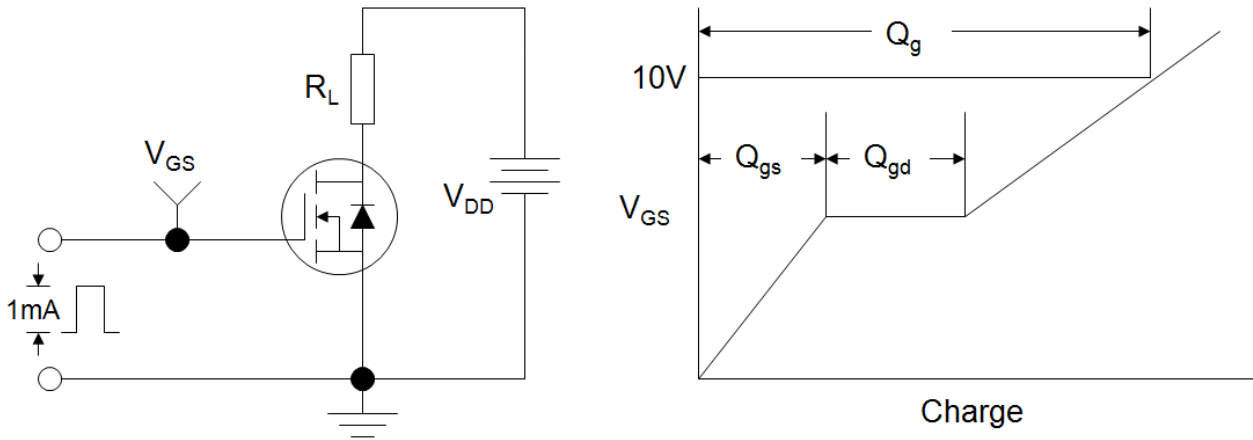


Figure B: Resistive Switching Test Circuit and Waveform

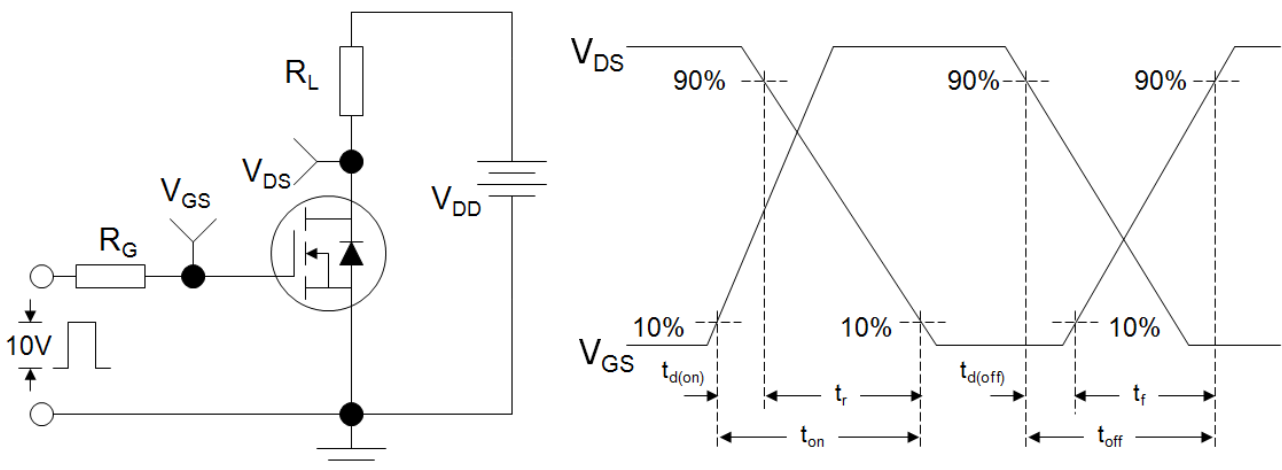
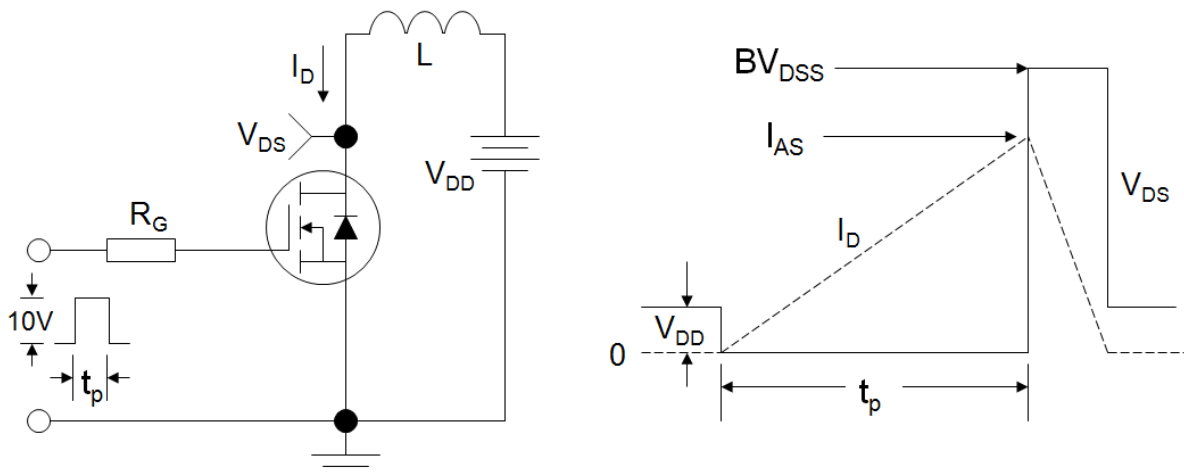
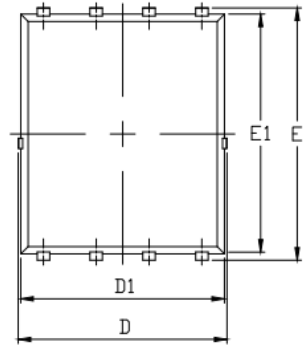


Figure C: Unclamped Inductive Switching Test Circuit and Waveform

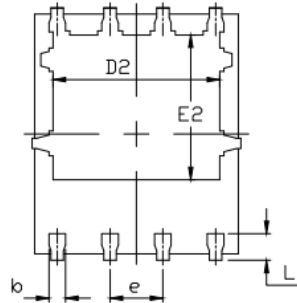


Package Information

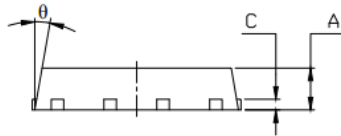
DFN5*6 package outline dimension



Top View



Bottom View



Side View

Power56			
DIM.	MIN.	MAX.	TYP.
A	0.95	1.05	1.00
b	0.30	0.50	0.40
C	0.254		
D	5.02		
D1	4.80	5.00	4.90
D2	3.91	4.11	4.01
E	5.95	6.15	6.05
E1	5.60	5.90	5.75
E2	3.38	3.58	3.48
e	1.27REF		
L	0.45	0.65	0.55
θ	10°		



Revision History

Revision	Subjects (major changes since last revision)	Date
1.0	Initial version	2020.3
2.0	RDS(on)max	2021.8